

ABSTRACT

A data processor that allows a CPU to access an external memory in an interval between data accesses from a DSP having a variable data length. In a case where a 24-bit mode is set, when a determination section determines that the DSP is accessing the external memory, a control section commands to place an access from the CPU to the external memory in a wait state. In a case where a 16-bit mode is set, the control section commands an address-data switching section, allowing the CPU to access the external memory by utilizing a third bus cycle, which is free.